

# **Audio 1-Chip SOC**

### **BM94803AEKU**

### **General Description**

BM94803AEKU is 1-Chip SOC for multimedia audio systems, which supports the USB memory, SD memory card, and CD. This IC has a built-in ARM946ES processor, SDRAM, and various peripherals. It is designated to download programs from external Serial Flash ROM and execute system control, file system management, Audio CODEC, and a wide range of media control.

BM94803AEKU supports USB High-Speed and has built-in DSD Native reproduction function.

### **Key Features**

This IC includes the following blocks:

### Processor

■ ARM946ES Microprocessor Core

#### Memory

- SDRAM
- Initial Program ROM
- Program SRAM
- Data SRAM
- SDRAM Controller

#### System

- Multilayer AHB
- Interrupt Controller
- DMA Controller

### Serial, Media I/F

- GPIO
- Pin Controller
- USB2.0 Dual Role(Host/Device) Controller
- SD I/F
- Quad SPI I/F
- SPI I/F (Master/Slave)
- I2C I/F (Master/Slave)
- UART I/F
- I2S Input I/F
- I2S Output I/F
- CD Servo Controllers
- CD-ROM Decoder
- General Purpose A/D Converter

### Timer

- Timer
- Watchdog Timer
- Real Time Clock

### Other

- Clock Generator
- Reset Generator
- PLL

### **Package**



### **Application**

Component Stereo

### **Application Block**

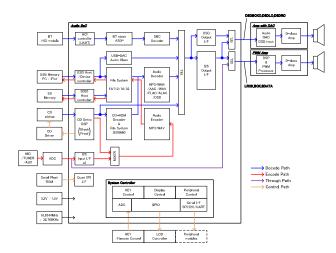


Figure 1. Application Block

#### Lineup

Туре	Package	Orderable Type	
BM94803AEKU	HTQFP128UA	Tray	BM94803AEKU-Z

## **Feature**

		BM94801KUT	BM94803AEKU	
	Package	TQFP128UM	HTQFP128UA	
	ARM946ES	96MHz	108MHz	
Processor	ICache/Dcache	4kB/4kB	4kB/4kB	
	SDRAM	16Mbit	16Mbit	
	Initial Program ROM	2kByte	2kByte	
Memory	Program SRAM	64kByte	64kByte	
	Data SRAM	64kByte	64kByte	
	Multilayer AHB	support	support	
System	Interrupt Controller	support	support	
	DMA Controller	2ch	1ch	
	GPIO	support	support	
	Pin Controller	support	support	
	USB2.0 Controller	HS 1port	HS 1port	
	SD I/F	1ch	1ch	
	Quad SPI I/F	1ch	1ch	
	SPI I/F (Master)	1ch	1ch	
	SPI I/F (Slave)	1ch	1ch	
	I2C I/F (Master/Slave)	2ch	2ch	
Periphera <b>l</b>	UART I/F	2ch	2ch	
<b>İ</b> /F	I2S Input I/F	2ch 2series	2ch 2series	
		I2S:stereo + mono	I2S:stereo	
	I2S Output I/F	192kHz/24bit	192kHz/24bit	
			DSD : 5.6448MHz	
	CD Servo Controllers	support	support	
	CD-ROM Decoder	support	support	
	RemoteControll	support	support	
	General purpose  A/D Converter	1.5V x 8ch	3.3V x 8ch	
	Timer	5ch	5ch	
Timer	Watchdog Timer	1ch	1ch	
	Real Time Clock	1ch	1ch	
	DSP	-	-	
Entertainment	PWM out	-	_	
Accelerator	FLAC/ALAC	_	-	
	Clock Generator	support	support	
Clock	Reset Generator	support	support	

Note: specification in the Datasheet is correct for the specifications of BM94801KUT.

### ARM946ES Microprocessor Core

- ♦ 32Bit RISC Processor
- ♦ Operating Frequency: 108MHz
- 8kByte Cache
   Data Cache 4kByte
   Instruction Cache 4kByte

### **SDRAM**

- ♦ 16Mbit
- ♦ SDRAM with built-in MSM56V16160N from LAPIS Semiconductor
- ♦ 2Bank x 524,288-word x 16Bit

### Initial Program ROM

- ♦ ITCM ROM Size: 2kByte (512Word x 32Bit)
- ♦ boot program
- ♦ No-wait access

#### REMAP

♦ Remapping can be implemented by writing to internal registers.

### SHADOW SRAM

- ♦ RAM Size: 512Byte (128-Word x 32-Bit)
- ♦ No-wait access

### Program SRAM

- ♦ ITCM RAM Size: 64kByte (16,384-Word x 32-Bit)
- ♦ No-wait access

#### Data SRAM

- ♦ DTCM RAM Size: 64kByte (16,384-Word x 32-Bit)
- ♦ No-wait access

### SDRAM Controller

- ♦ Supports SDRAM
- Supports 11Bit row address, 8-bit column address, and 1-bit bank address to SDRAM

### **AMBA**

- ♦ 32Bit Data Bus
- ♦ Arbitrates ARM and DMA access with an arbiter

### Interrupt Controller

- ♦ 1 FIQ Interrupt Line
- Allows programmable setting of interrupt priority levels
- Allows setting of 16 vector addresses

### **DMA Controller**

- ♦ Channel FIFO Depth Up to 16 Bytes
- ♦ Allows programmable setting of transfer data width in the range of 1Byte to 4Bytes
- Allows programmable setting of channel priority levels
- ♦ Maximum Block Length Up to 4,095 Words
- Includes 12 handshake interfaces available for assignment to channels with software
- ♦ Supports multiblock transfers
- ♦ Connects the master board to system bus

### **GPIO**

- ♦ GPIO0(32 pins), GPIO1(32 pins), GPIO2(13pins)
  - 4 of 17 pins assigned GPIO2 are not available because of analog pin. (See P9 Pin Description)
- Supports a maximum of 77 I/O pins (including 13 GPIO pins for exclusive use)
- ♦ Supports the interrupt function
- ♦ Supports external level-sensitive interrupt

#### Pin Controller

♦ Controls connection settings between pins and blocks

#### USB2.0 Dual Role (Host/Device) controller

- ♦ USB 2.0 conformance
- ♦ Bit rate: High-Speed (480Mbps)/Full-Speed (12Mbps)
- ♦ Configurable for up to five transmit endpoint FIFOs and four receive endpoint FIFOs (including endpoint 0)
- Each endpoint FIFO supports bulk transfer, interrupt transfer, and isochronous transfer.
- ♦ 4096-Byte RAM for Endpoint FIFO

### SD I/F

- ♦ Supports SDHC, and SD cards
- Provide access to SD card in SD Bus mode
- ♦ Allows control from the AMBA-AHB Bus
- ♦ Includes 512 Byte data transmit/receive FIFOs

### Quad SPI I/F

- ♦ Supports quad serial flash ROM
- ♦ Supports serial flash ROM address up to 24 bits
- ♦ Allows the setting of control registers from the AMBA-AHB bus
- Allows direct access from the memory map of the AMBA-AHB bus to serial flash ROM
- ♦ Includes 32 byte transmit/receive FIFOs

### SSI Master

- ♦ FIFO Depth Up to 16 Words and FIFO Data Width Up to 16Bits
- ♦ Selectable Data Size from 4 Bits to 16 Bits
- ♦ Serial protocol supports SPI from Motorola
- ♦ Includes DMA handshake interface

### SSI Slave

- ♦ FIFO Depth Up to 16 Words and FIFO Data Width Up to 16 Bits
- ♦ Selectable Data Size from 4 Bits to 16 Bits
- ♦ Serial protocol supports SPI from Motorola
- ♦ Includes DMA handshake interface

### I2C I/F (Master/Slave)

- ♦ 2 Ch I2C Serial Interface
- ♦ Supports two speed modes
- ♦ Standard mode (100Kb/s)
- → Fast mode (400Kb/s)
- ♦ Supports I2C Master and Slave operation
- ♦ Allows 7 and 10 bit address generation
- Has built-in 32 stage transmit and receive FIFOs
- ♦ Includes DMA handshake interface

### UART I/F

- ♦ IS16550-Based
- Allows various baud rate settings with software (up to 6Mbps)
- ♦ No Support for IrDA
- ♦ FIFO Depth Up to 32 Words and FIFO Data Width Up to 8 Bits
- ♦ Incorporates a function to invert output
- ♦ Includes DMA handshake interface

#### I2S Input I/F

- ♦ Two Lines of 2-Ch Digital Audio Input
- ♦ I2S, EIAJ format
- ♦ 16-Bit Data
- ♦ Selectable Bit Clock from 32fs, 48fs, and 64fs
- ♦ Selectable Input Sample Rate from 32kHz, 44.1kHz, and 48kHz
- ♦ One Line of Internal Input from the CD Servo Controller
- ♦ Maximum Input Rate Up to 4x
- ♦ Supports detection of CD-DA link
- ♦ Supports detection of CD-ROM sync
- ♦ Supports CD-ROM data descrambling
- ♦ Acquires Sub-Q data
- Acquires CD-Text data
- ♦ Built-in DMA 2ch
- ♦ Supports I2S Input at CD Play

#### I2S Output I/F

- ♦ 2-Ch Digital Audio Output x 1 ( 2ch from Decoder)
- ♦ I2S, EIAJ format
- ♦ Selectable PCM Output Sample Rate from 32k, 44.1k, 48k, 88.2k, 96k,176.4k,192kHz
- ♦ Selectable PCM Data Width from 16 and 24 bits
- ♦ 64 fs PCM Bit Clock
- ♦ Supports pitch control (x0.5 x2.0, 25step)
- Selectable DSD Output Sample Rate from DSD 2.8224MHz, 5.6448MHz

#### CD servo controller

- ♦ Supports rotation speed of CD up to 4x
- Built-in Preservo-Amplifier with Power Save Mode, which supports Playback of CD-RW
- ♦ Allows independent offset adjustment of AC, BD, E, and F amplifiers
- ♦ Built-in Auto-Tracking and Focus Adjustment Function
- ♦ Built-in PLL and CLV with a Wide Lock Range
- ♦ Built-in Asymmetry Correction Function

### **CD-ROM Decoder**

- ♦ Supports Mode1, Mode2 form1, Mode2 form2
- ♦ Supports ECC, EDC
- ♦ Built-in DMA

#### General Purpose A/D Converter

- ♦ 10-Bit SAR ADC, 8 Ch ADC
- ♦ Analog Input Voltage range: VDD\_ADC x10% to VDD\_ADC x 90%
- ♦ Maximum A/D Conversion frequency Ch=88.2ksps

#### Timer

- Supports five independent programmable timer functions
- ♦ Each timer supports time width up to 32 bits
- ♦ Each timer supports independent interrupt signal

### Watchdog Timer

- ♦ Composed of a counter having a set cycle to monitor the occurrence of timeout event
- ♦ Counter Width Up to 32 Bits
- The counter counts down from the set value and sets timeout occurrence when it reaches zero

### Realtime clock

- ♦ 32 Bit Programmable Timer
- ♦ Supports interrupt signals
- ♦ External 32.768 kHz Crystal Oscillator

### Remote Controller Receiver (RCR)

- ♦ Converts infrared remote control signal to code
- Compatible with the signal format of the Association for Electric Home Appliances
- ♦ Supports Sony format
- Enables to setup permissible value of input signal cycle to adjust the Duty deviation of input signal

### Clock Generator

- Supplies clocks to individual internal blocks
- ♦ Allows on/off control of clocks to individual blocks
- ♦ Generates master audio clocks
- ♦ At the normal operation, supports three modes (High-Speed mode, Middle Speed mode, Low-Speed mode)
- ♦ Supports Standby Mode

### Reset Generator

♦ Generates a pulse to be supplied to individual blocks

#### PLL

- ♦ Generates 216MHz / 240MHz clock used to generate system clocks
- ♦ Generates 135.4752 MHz and 147.456 MHz clocks used to generate audio clocks

### Power Supply Voltage

- ♦ I/O Power Supply Voltage : 3.3V(3.0V to 3.6V)
- Analog Power Supply Voltage: 3.3V(3.0V to 3.6V)
   (Used for SDRAM, CD servo, USB, and ADC)
- Osed for SDIVAM, CD servo, OSB, and ADC)
   Digital Core Power Supply Voltage : 1.5V(1.45V to 1.65V)
   (Used for Digital Core)

### **Pin Assignment**

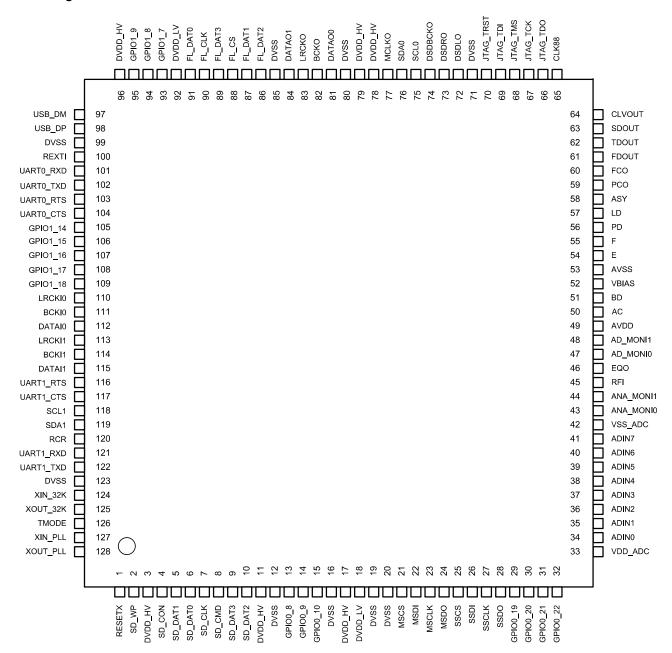


Figure 2. Pin Assignment

Pin Description

No	Pin De	scription				
1			Pin Name	GPIO	I/O	Function
SD			<del></del>			
3				GPIO0f01		
SD				Gi (Oo[o]	-	
SD				CDIO0141	1/0	
6 SD   SD DATO   GPIO(3]   I/O   SD Card I/F Data I/O (0)						
SD						
SD						
9   SD   SD   DAT2   GPI00[6]   I/O   SD   Card I/F Data I/O (2)						
10   SD						
11   POWER   DVD   HV						
12				GPI00[7]	I/O	SD Card I/F Data I/O (2)
13   GPIO	11	POWER	DVDD_HV		-	3.3V Power Supply
14	12	POWER	DVSS		-	GND
14	13	GPIO	GPIO0 8	GPIO0[8]	I/O	GPIO for exclusive use
15   GPIO   GPIO_10   GPIO0_110   I/O   OPEN/CLOSE detect pin of CD mechanical tray.		0010	_			GPIO pin. When CD is used, this pin is TRAY
15   GPIO	14	GPIO	GPIO0_9	GPI00[9]	I/O	
16	15	GPIO	GPIO0 10	GPIO0[10]	I/O	
17				O. 100[10]		
18						
19						
Down						
MSIO					-	
22 MSIO				001001441		
23						
24						
25						
26         SSIO         SSDI         GPIO0[16]         I/O         SIO Slave Data Input           27         SSIO         SSCLK         GPIO0[17]         I/O         SIO Slave Data Dutput           28         SSIO         SSDO         GPIO0[18]         I/O         SIO Slave Data Output           29         GPIO         GPIO0_19         GPIO0[19]         I/O         GPIO for exclusive use           30         GPIO         GPIO0_21         GPIO0[21]         I/O         GPIO for exclusive use           31         GPIO         GPIO0_21         GPIO0[22]         I/O         GPIO for exclusive use           32         GPIO         GPIO0_22         GPIO0[22]         I/O         GPIO for exclusive use           33         POWER         VDD ADC        3.3 V ADC Power Supply           34         ADC         ADINO         GPIO2[0]         I AD input CHO or GPIO           35         ADC         ADIN1         GPIO2[1]         I AD input CH1 or GPIO           36         ADC         ADIN3         GPIO2[2]         I AD input CH3 or GPIO           38         ADC         ADIN4         GPIO2[3]         I AD input CH4 or GPIO           40         ADC         ADIN6         GPIO2[6]						
27	25					SIO Slave Chip Select Input
28         SSIO         SSDO         GPIO0[18]         I/O         SIO Slave Data Output           29         GPIO         GPIO0_19         GPIO0[19]         I/O         GPIO for exclusive use           30         GPIO         GPIO0_20         GPIO0[20]         I/O         GPIO for exclusive use           31         GPIO         GPIO0_21         GPIO0[21]         I/O         GPIO pin. When CD is used, this pin is INNER_SW detect pin.           32         GPIO         GPIO0_22         GPIO0[22]         I/O         GPIO for exclusive use           33         POWER         VDD_ADC         -         3.3V ADC Power Supply           34         ADC         ADIN0         GPIO2[0]         I         AD input CH0 or GPIO           35         ADC         ADIN1         GPIO2[1]         I         AD input CH1 or GPIO           36         ADC         ADIN3         GPIO2[3]         I         AD input CH2 or GPIO           37         ADC         ADIN3         GPIO2[3]         I         AD input CH4 or GPIO           38         ADC         ADIN6         GPIO2[4]         I         AD input CH3 or GPIO           40         ADC         ADIN6         GPIO2[6]         I         AD input CH6 or GPIO </td <td>26</td> <td>SSIO</td> <td>SSDI</td> <td>GPIO0[16]</td> <td></td> <td>SIO Slave Data Input</td>	26	SSIO	SSDI	GPIO0[16]		SIO Slave Data Input
Page   Page	27	SSIO	SSCLK	GPIO0[17]	I/O	SIO Slave Clock Input
Page   Page	28	SSIO	SSDO	GPI00[18]	I/O	SIO Slave Data Output
30 GPIO						
GPIO	30					
31   GPIO   GPIO0_21   GPIO0[21]   I/O   pin.     32   GPIO   GPIO0_22   GPIO0[22]   I/O   GPIO for exclusive use     33   POWER   VDD_ADC   - 3.3V ADC Power Supply     34   ADC   ADIN0   GPIO2[0]   I   AD input CH0 or GPIO     35   ADC   ADIN1   GPIO2[1]   I   AD input CH1 or GPIO     36   ADC   ADIN2   GPIO2[2]   I   AD input CH2 or GPIO     37   ADC   ADIN3   GPIO2[3]   I   AD input CH3 or GPIO     38   ADC   ADIN4   GPIO2[4]   I   AD input CH4 or GPIO     39   ADC   ADIN5   GPIO2[5]   I   AD input CH5 or GPIO     40   ADC   ADIN5   GPIO2[6]   I   AD input CH6 or GPIO     41   ADC   ADIN6   GPIO2[6]   I   AD input CH6 or GPIO     41   ADC   ADIN7   GPIO2[7]   I   AD input CH7 or GPIO     42   POWER   VSS_ADC   - ADC_GND     43   CDDSP   ANA MONI0   GPIO2[8]   I/O   Input & Analog Monitor Output or GPIO     44   CDDSP   ANA MONI1   GPIO2[9]   I/O   Input & Analog Monitor Output or GPIO     45   CDDSP   EQO   O Output RF Equalizer     46   CDDSP   AD MONI0   GPIO2[10]   I/O   Input & Monitor Signal Output or GPIO     48   CDDSP   AD MONI1   GPIO2[11]   I/O   Input & Monitor Signal Output or GPIO     48   CDDSP   AD MONI1   GPIO2[11]   I/O   Input & Monitor Signal Output or GPIO     49   POWER   AVDD   - 3.3V CD RF Power Supply     50   CDDSP   AC   I   A + C Voltage Input     51   CDDSP   BD   I   B + D Voltage Input     52   CDDSP   F   I   F Voltage Input     53   CDDSP   F   I   F Voltage Input     54   CDDSP   F   I   APC Photo Detector Input						
32   GPIO   GPIO0_22   GPIO0[22]   I/O   GPIO for exclusive use	31	GPIO	GPIO0_21	GPIO0[21]	I/O	· · · · · · —
33	32	GPIO	GPION 22	GPI00[22]	I/O	
34   ADC   ADINO   GPIO2[0]   I   AD input CH0 or GPIO				Or IOU[ZZ]		
35   ADC   ADIN1   GPIO2[1]   I   AD input CH1 or GPIO				CDIO3[0]		
36         ADC         ADIN2         GPIO2[2]         I         AD input CH2 or GPIO           37         ADC         ADIN3         GPIO2[3]         I         AD input CH3 or GPIO           38         ADC         ADIN4         GPIO2[4]         I         AD input CH4 or GPIO           39         ADC         ADIN5         GPIO2[5]         I         AD input CH5 or GPIO           40         ADC         ADIN6         GPIO2[6]         I         AD input CH6 or GPIO           41         ADC         ADIN7         GPIO2[7]         I         AD input CH6 or GPIO           41         ADC         ADIN7         GPIO2[7]         I         AD input CH6 or GPIO           41         ADC         ADIN7         GPIO2[7]         I         AD input CH6 or GPIO           42         POWER         VSS_ADC         -         ADC GND           43         CDDSP         ANA_MONIO         GPIO2[8]         I/O         Input & Analog Monitor Output or GPIO           44         CDDSP         ANA_MONIO         GPIO2[9]         I/O         Input & Analog Monitor Output or GPIO           45         CDDSP         AD_MONIO         GPIO2[10]         I/O         Input & Monitor Signal Output or GPIO					•	
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44       CDDSP       ANA MONI1       GPIO2[9]       I/O       Input & Analog Monitor Output or GPIO         45       CDDSP       RFI       I RF Output Capacitance Coupling Re-Input         46       CDDSP       EQO       O Output RF Equalizer         47       CDDSP       AD MONI0       GPIO2[10]       I/O Input & Monitor Signal Output or GPIO         48       CDDSP       AD MONI1       GPIO2[11]       I/O Input & Monitor Signal Output or GPIO         49       POWER       AVDD       - 3.3V CD RF Power Supply         50       CDDSP       AC       I A + C Voltage Input         51       CDDSP       BD       I B + D Voltage Input         52       CDDSP       VBIAS       O VBIAS Output         53       POWER       AVSS       - CD RF GND         54       CDDSP       E       I E Voltage Input         55       CDDSP       F       I F Voltage Input         56       CDDSP       PD       I APC Photo Detector Input	43	CDDSP	ANA_MONI0	GPIO2[8]	I/O	Input & Analog Monitor Output or GPIO
A5   CDDSP   RFI     I   RF Output Capacitance Coupling Re-Input	44				I/O	
46         CDDSP         EQO         O         Output RF Equalizer           47         CDDSP         AD_MONI0         GPIO2[10]         I/O         Input & Monitor Signal Output or GPIO           48         CDDSP         AD_MONI1         GPIO2[11]         I/O         Input & Monitor Signal Output or GPIO           49         POWER         AVDD         -         3.3V CD RF Power Supply           50         CDDSP         AC         I         A + C Voltage Input           51         CDDSP         BD         I         B + D Voltage Input           52         CDDSP         VBIAS         O         VBIAS Output           53         POWER         AVSS         -         CD RF GND           54         CDDSP         E         I         E Voltage Input           55         CDDSP         F         I         F Voltage Input           56         CDDSP         PD         I         APC Photo Detector Input					I	
47         CDDSP         AD_MONI0         GPIO2[10]         I/O         Input & Monitor Signal Output or GPIO           48         CDDSP         AD_MONI1         GPIO2[11]         I/O         Input & Monitor Signal Output or GPIO           49         POWER         AVDD         -         3.3V CD RF Power Supply           50         CDDSP         AC         I         A + C Voltage Input           51         CDDSP         BD         I         B + D Voltage Input           52         CDDSP         VBIAS         O         VBIAS Output           53         POWER         AVSS         -         CD RF GND           54         CDDSP         E         I         E Voltage Input           55         CDDSP         F         I         F Voltage Input           56         CDDSP         PD         I         APC Photo Detector Input					0	
48         CDDSP         AD_MONI1         GPIO2[11]         I/O         Input & Monitor Signal Output or GPIO           49         POWER         AVDD         - 3.3V CD RF Power Supply           50         CDDSP         AC         I A + C Voltage Input           51         CDDSP         BD         I B + D Voltage Input           52         CDDSP         VBIAS         O VBIAS Output           53         POWER         AVSS         - CD RF GND           54         CDDSP         E         I E Voltage Input           55         CDDSP         F         I F Voltage Input           56         CDDSP         PD         I APC Photo Detector Input				GPI02[10]		
49         POWER         AVDD         - 3.3V CD RF Power Supply           50         CDDSP         AC         I A + C Voltage Input           51         CDDSP         BD         I B + D Voltage Input           52         CDDSP         VBIAS         O VBIAS Output           53         POWER         AVSS         - CD RF GND           54         CDDSP         E         I E Voltage Input           55         CDDSP         F         I F Voltage Input           56         CDDSP         PD         I APC Photo Detector Input						
50         CDDSP         AC         I         A + C Voltage Input           51         CDDSP         BD         I         B + D Voltage Input           52         CDDSP         VBIAS         O         VBIAS Output           53         POWER         AVSS         -         CD RF GND           54         CDDSP         E         I         E Voltage Input           55         CDDSP         F         I         F Voltage Input           56         CDDSP         PD         I         APC Photo Detector Input				J. 132[11]		
51         CDDSP         BD         I         B + D Voltage Input           52         CDDSP         VBIAS         O         VBIAS Output           53         POWER         AVSS         -         CD RF GND           54         CDDSP         E         I         E Voltage Input           55         CDDSP         F         I         F Voltage Input           56         CDDSP         PD         I         APC Photo Detector Input						
52         CDDSP         VBIAS         O         VBIAS Output           53         POWER         AVSS         -         CD RF GND           54         CDDSP         E         I         E Voltage Input           55         CDDSP         F         I         F Voltage Input           56         CDDSP         PD         I         APC Photo Detector Input					<u> </u>	
53         POWER         AVSS         -         CD RF GND           54         CDDSP         E         I         E Voltage Input           55         CDDSP         F         I         F Voltage Input           56         CDDSP         PD         I         APC Photo Detector Input		CDDSP				
54         CDDSP         E         I         E Voltage Input           55         CDDSP         F         I         F Voltage Input           56         CDDSP         PD         I         APC Photo Detector Input						
55     CDDSP     F     I     F Voltage Input       56     CDDSP     PD     I     APC Photo Detector Input					-	
56 CDDSP PD I APC Photo Detector Input					<u> </u>	E Voltage Input
57   CDDSP   LD   O   APC Laser Drive Output					J	
	57	CDDSP	LD		0	APC Laser Drive Output

Pin De	escription – c	continued			
No	Block	Pin Name	GPIO	I/O	Function
58	CDDSP	ASY		I	Asymmetric Correction
59	CDDSP	PCO		0	PLL PCO Output
60	CDDSP	FCO		0	PLL FCO-DAC Output
61	CDDSP	FDOUT	CDIO3[43]	I/O	Focus Drive Output
01	CDDSP	FDOOT	GPIO2[12]	1/0	Use this pin as analog pin.
62	CDDSP	TDOUT	CDIO3[13]	I/O	Tracking Drive Output
02	CDDSP	10001	GPIO2[13]	1/0	Use this pin as analog pin.
63	CDDSP	SDOUT	GPIO2[14]	I/O	Sled Drive Output
03	CDDSF	30001	GF102[14]	1/0	Use this pin as analog pin.
64	CDDSP	CLVOUT	GPIO2[15]	I/O	CLV Drive Output
					Use this pin as analog pin.
65	CDDSP	CLK88	GPIO2[16]	I/O	Clock Output for Driver IC or GPIO
66	JTAG	JTAG_TDO		0	JTAG TDO
67	JTAG	JTAG_TCK			JTAG TCK
68	JTAG	JTAG_TMS			JTAG TMS
69	JTAG	JTAG_TDI			JTAG TDI
70	JTAG	JTAG_TRST		I/O	JTAG TRST
71	POWER	DVSS		-	GND
72	DSD/GPIO	DSDLO	GPI00[23]	I/O	DSD Lch Data Output or GPIO
73	DSD/GPIO	DSDRO	GPI00[24]	I/O	DSD Rch Data Output or GPIO
74	DSD/GPIO	DSDBCKO	GPIO0[25]	I/O	DSD Bit Clock Output or GPIO
75	I2C	SCL0	GPIO0[26]	I/O	I2C Clock I/O (0), Open drain output pin
76	I2C	SDA0	GPI00[27]	I/O	I2C Data I/O (0), Open drain output pin
77	I2S OUT	MCLKO	GPI00[28]	I/O	Digital Audio Master Clock Output
78	POWER	DVDD_HV		-	3.3V Power Supply
79	POWER	DVDD_HV		-	3.3V Power Supply
80	POWER	DVSS	OBLOSIOSI	-	GND
81	I2S OUT	DATAO0	GPI00[29]	I/O	Digital Audio Data Output (0)
82	I2S OUT	BCKO	GPI00[30]	I/O	Digital Audio Bit Clock Output
83	I2S OUT	LRCKO	GPI00[31]	I/O	Digital Audio Channel Clock Output
84	I2S OUT	DATAO1	GPIO1[0]	I/O	Digital Audio Data Output (1)
85	POWER	DVSS	ODIO4141	I/O	GND
86	FLASH	FL_DAT2	GPIO1[1] GPIO1[2]		Serial Flosh ROM IF Data I/O (2)
87	FLASH	FL_DAT1		1/0	Serial Flash ROM I/F Data I/O (1)
88 89	FLASH FLASH	FL_CS FL_DAT3	GPIO1[3]	I/O I/O	Serial Flash ROM I/F Command Output Serial Flash ROM I/F Data I/O (3)
90	FLASH	FL_DATS	GPIO1[4] GPIO1[5]	I/O	Serial Flash ROM I/F Clock Output
91	FLASH	FL_CLK FL DAT0	GPIO1[6]	1/0	Serial Flash ROM I/F Data I/O (0)
92	POWER	DVDD LV	GFIOT[0]		1.5V Power Supply
93	GPIO	GPIO1 7	GPIO1[7]	I/O	GPIO for exclusive use
93	GPIO	GPIO1_7 GPIO1_8	GPIO1[7] GPIO1[8]	I/O	GPIO for exclusive use
95	GPIO	GPIO1_8	GPIO1[8]	1/0	GPIO for exclusive use
96	POWER	DVDD_HV	GFIOT[8]	-	3.3V Power Supply
97	USB	USB DM		I/O	USB D-
98	USB	USB_DP		1/0	USB D+
99	POWER	DVSS		-	GND
33	· OVVLIX	5 7 0 0	+	_	USB Reference Voltage Output. Connect a pull down
					resistance to DVSS pin. The pull down resistance must be
				_	12.3 k $\Omega$ ±1%.
100	USB	REXTI		I	About on PCB, do not wire as long as possible and not wire
					side by side long distance with noise line, especially note
					the next pin UARTO RXD(pin101).
	1	1	1		

Pin Description - continued

Pin De	escription - co	ontinued			
No	Block	Pin Name	GPIO	I/O	Function
101	UART	UART0_RXD	GPIO1[10]	I/O	UART0 Receive Data
102	UART	UART0_TXD	GPIO1[11]	I/O	UART0 Transmit Data
103	UART	UART0_RTS	GPIO1[12]	I/O	UART0 Transfer Request
104	UART	UARTO_CTS	GPIO1[13]	I/O	UART0 Clear Request
105	GPIO	GPIO1_14	GPIO1[14]	I/O	GPIO for exclusive use
106	GPIO	GPIO1_15	GPIO1[15]	I/O	GPIO for exclusive use
107	GPIO	GPIO1_16	GPIO1[16]	I/O	GPIO for exclusive use
108	GPIO	GPIO1_17	GPIO1[17]	I/O	GPIO for exclusive use
109	GPIO	GPIO1_18	GPIO1[18]	I/O	GPIO for exclusive use
110	I2S IN	LRCKI0	GPIO1[19]	I/O	Digital Audio Channel Clock Input (0)
111	I2S IN	BCKI0	GPIO1[20]	I/O	Digital Audio Bit Clock Input (0)
112	I2S IN	DATA <b>I</b> 0	GPIO1[21]	I/O	Digital Audio Data Input (0)
113	I2S IN	LRCKI1	GPIO1[22]	I/O	Digital Audio Channel Clock Input (1)
114	I2S IN	BCKI1	GPIO1[23]	I/O	Digital Audio Bit Clock Input (1)
115	I2S IN	DATAI1	GPIO1[24]	I/O	Digital Audio Data Input (1)
116	UART	UART1_RTS	GPIO1[25]	I/O	UART1 Transfer Request
117	UART	UART1_CTS	GPIO1[26]	I/O	UART1 Clear Request
118	I2C	SCL1	GPIO1[27]	I/O	I2C Clock I/O (1), Open drain output pin
119	I2C	SDA1	GPIO1[28]	I/O	I2C Data I/O (1), Open drain output pin
120	RCR	RCR	GPIO1[29]	I/O	Remote Controller Signal Input
121	UART	UART1_RXD	GPIO1[30]	I/O	UART1 Receive Data
122	UART	UART1_TXD	GPIO1[31]	I/O	UART1 Transmit Data
123	POWER	DVSS		-	GND
124	CLOCK	XIN_32K			X'tal(32.768KHz) connection input pin.
125	CLOCK	XOUT_32K		0	X'tal(32.768KHz) connection output pin.
126	TEST	TMODE			Test Mode pin: This pin is connected to GND.
127	CLOCK	XIN_PLL			X'tal(16.9344MHz) Connection Input
128	CLOCK	XOUT_PLL		0	X'tal(16.9344MHz) Connection Output

### **Application Circuit Diagram**

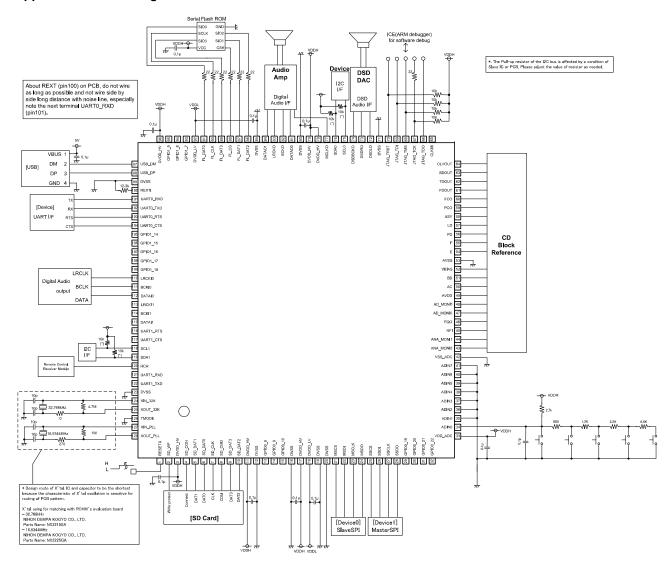


Figure 3. Application Circuit Diagram

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Remarks
Input Voltage (Analog, I/O)	VDDHMAX	-0.3 to +4.5	V	DVDD_HV, VDD_ADC, AVDD
Input Voltage (Core)	VDDLMAX	-0.3 to +2.1	V	DVDD_LV
Input Voltage	VIN	-0.3 to VDDH+0.3	V	
Storage Temperature Range	TSTG	-55 to +125	°C	
Operating Temperature Range	TOPR	-40 to +85	°C	
Maximum Junction Temperature	Tjmax	+125	°C	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating	Unit	Remarks
Input Voltage (Analog, I/O)	VDDH	3.0 to 3.6	V	DVDD_HV, VDD_ADC, AVDD
Input Voltage (Core)	VDDL	1.45 to 1.65	V	DVDD_LV

# Thermal Resistance (Note 1)

Devenotor	Curahal	Thermal Res	1.1:4		
Parameter	Symbol	1s (Note 3)	2s2p (Note 4)	Unit	
HTQFP128UA					
Junction to Ambient	$\theta_{JA}$	54.9	27.6	°C/W	
Junction to Top Characterization Parameter <sup>(Note 2)</sup>	$\Psi_{JT}$	10	9	°C/W	

<sup>(</sup>Note 1) Based on JESD51-2A(Still-Air)

<sup>(</sup>Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt
Тор		
Copper Pattern	Thickness	
Footprints and Traces	70µm	

Layer Number of	Material	Board Size		Thermal Via (Note 5)		
Measurement Board	iviateriai	Doard Size		Pitch	Diameter	
4 Layers	FR-4	114.3mm x 76.2mm	x 1.6mmt	1.20mm	Ф0.30mm	
Тор	Тор		ers	Bottom		
Copper Pattern	Thickness	Copper Pattern Thickness		Copper Pattern	Thickness	
Footprints and Traces	70µm	74.2mm (Square)	35µm	74.2mm (Square	70µm	

<sup>(</sup>Note 5) This thermal via connects with the copper pattern of all layers.

Caution: As reference information of thermal design, thermal resistance of 1s and 2s2p are described. If the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. Increase the board size and copper area to prevent exceeding the maximum junction temperature rating. This IC is recommended more than 2s PCB.

<sup>(</sup>Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

<sup>(</sup>Note 3) Using a PCB board based on JESD51-3.

### **Electrical Characteristics**

 $(Unless\ otherwise\ noted,\ Ta=25^{\circ}C,\ DVDD\_HV\ =\ VDD\_ADC\ =\ AVDD\ =\ 3.0V,\ DVDD\_LV\ =\ 1.5V,\ DVSS=VSS\_ADC=AVSS$ =0V, XIN PLL= 16.9344MHz, XIN 32K =32.768kHz, REXTI pin externally fitted resistance = 12.3 k $\Omega$ ±1%)

		=32.768kHz, REXTI pin externally f				Conditions	
Parameter	Symbol	MIN	TYP	MAX	Unit	Suitable Pin	
<overall></overall>		•				,	
Operating Current Consumption (VDDH)	IDDHS1	-	115	180	mA	Using USB High-Speed	
Operating Current Consumption (VDDL)	IDD2	-	150	210	mA		
In a standby mode Consumption current (VDDH)	ISTBH	-	1.1	-	mA	At standby mode	
In a standby mode Consumption current (VDDL)	ISTBL	-	50	ı	μΑ	At standby mode	
<logic interface=""></logic>						- (Nata 4)	
H input current	IIH	-	-	1.0	μΑ	(Note 1)	
L input current	IIL	-1.0	-	-	μΑ	(Note 1)	
Input "H" Voltage	VIH	VDDH*0.7	-	VDDH	V	(Note 1)	
Input "L" Voltage	VIL	DVSS	-	VDDH*0.3	V	(Note 1)	
Output "H" Voltage 1	VOH1	VDDH-0.4	-	VDDH	V	IOH=-1.6mA, (Note 2)	
Output "L" Voltage 1	VOL1	0	-	0.4	V	IOL=1.6mA. (Note 2)	
Output "H" Voltage 2	VOH2	VDDH-0.4	-	VDDH	V	IOH=-3.6mA, (Note 3)	
Output "L" Voltage 2	VOL2	0	-	0.4	V	IOL=3.6mA. (Note 3) (Note 4)	
Output "H" Voltage 3	VOH3	VDDH-1.0	-	VDDH	V	IOH=-0.6mA, (Note 5)	
Output "L" Voltage 3	VOL3	0	-	1.0	V	IOL=0.6mA, (Note 5)	
<usb interface=""></usb>						,	
Idle Pull-Up Resistance	RPU ID	0.9	_	1.575	kΩ	(Note 7)	
RX Pull-Up Resistance	RPU RX	1.425	-	3.09	kΩ	(Note 7)	
Pull-Down Resistance	RPD	14.25	_	24.8	kΩ	(Note 6)	
HS High Voltage	VHSOH	360	_	440	mV	(Note 6)	
HS RX Differential Input				440		(Note 6)	
Sensitivity	VHSSQ	100	-	-	mV	(Note 0)	
HS RX Differential Input Range	VHSCM	-50	-	600	mV	(Note 6)	
HS Disconnect Judgment Voltage	VHSDSC	525	-	625	mV	(Note 6)	
Chirp J Voltage	VCHIRPJ	700	-	1100	mV	Measured at $45\Omega$ Output Termination (Note 6)	
Chirp K Voltage	VCHIRPK	-900	-	-500	mV	(Note 6)	
FS High Output Impedance	ZFDRH	-	45	-	Ω	(Note 6)	
FS Low Output Impedance	ZFDRL	_	45	_	Ω	(Note 6)	
FS High Voltage	VFOH	2.8	-	3.6	V	Measured when pin is pulled down to VSS using 15 kΩ resistor (Note 6)	
FS Low Voltage	VFOL	0	-	0.3	V	Measured when pin is pulled up to DVDD HV using 1.5 k $\Omega$ resistor (Note 6)	
FS RX Differential Input Sensitivity	VFLSNS	-	-	200	mV	(Note 6)	
FS RX Differential Input Range	VFLCM	0.8	-	2.5	V	(Note 6)	
H input voltage	VIHUSB	2	-	VDDH	V	(Note 6)	
L input voltage	VILUSB	DVSS	-	0.8	V	(Note 6)	
<adc></adc>	555		1	5.0	•		
A/D Conversion Frequency	FADCONV	_	-	705.6	kHz	FADCONV≤16.9344MHz/24	
Analog Input Voltage Range	VAIN	0.1*VDDH	-	0.9*VDDH	V		
Differential Non-Linearity	DNL	-	-	±5	LSB		
Integral Non-Linearity	INL			±5	LSB		
integral Non-Linearity	IINL	-	-	ΞЭ	LOD	1	

<sup>(</sup>Note 1) Input pin 1,2,4-10,13-15,21-32,34-41,43-44,47-48,65,67-70,72-77,81-84,86-91,93-95,101-122 pin

<sup>(</sup>Note 2) Output pin1 13-15,29-32,34-41,43,44,47,48,61-66,77,81-84,93-95,101-117,120-122 pin

<sup>(</sup>Note 3) Output pin2 2,4-10,21-28,72-74,86-91 pin

<sup>(</sup>Note 4) Output pin3 75,76,118,119 pin

<sup>(</sup>Note 5) Output pin4 125,128 pin

<sup>(</sup>Note 6) USB pin 97,98 pin

<sup>(</sup>Note 7) USB pin 98 pin

# **Electrical Characteristics – continued**

(Unless otherwise noted, Ta=25°C, DVDD\_HV = VDD\_ADC = AVDD = 3.0V, DVDD\_LV = 1.55V, DVSS= VSS\_ADC= AVSS= 0V, XIN\_PLL= 16.9344MHz, XIN\_32K =32.768kHz, RL=10kΩ, VBIAS=Reference)

0V, XIN_PLL= 16.934		K =32.768	Rating	JK12, VBIAS		Conditions
Parameter	Symbol	MIN	TYP	MAX	Unit	Suitable Pin
<pll (vco)="" block=""></pll>						
Maximum Oscillation Frequency	fVCOH	4.6	6.5	-	MHz	GPIO1_7,1/4 of VCO Output
Minimum Oscillation Frequency	fVCOL	-	1.1	1.7	MHz	GPIO1_7,1/4 of VCO Output
<fc dac=""> Offset Voltage</fc>	VFCOF	<b>-</b> 50	_	+50	mV	FCO
Maximum Output Voltage	VFCH	0.2	0.5	-	V	FCO
Minimum Output Voltage	VFCL	-	-0.5	-0.2	V	FCO
<pco.></pco.>						
Output "L" Voltage	VPCH	-	-1.0	-0.6	V	PCO
Output "H" Voltage	VPCL	0.6	1.0	-	V	PCO
< EFM Comparator >						
Threshold Voltage <servo adc=""></servo>	VEFM	<b>-</b> 200	-	200	mV	RFI,ANA_MONI0,GPIO1_8
Offset Voltage	VADOF	-140	_	+140	mV	ANA MONIO,ANA MONI1
Maximum Conversion Voltage	VADH	1.0	1.2	1.4	V	ANA_MONI0,ANA_MONI1
Minimum Conversion Voltage	VADL	-1.4	-1.2	-1.0	V	ANA_MONI0,ANA_MONI1
<servo dac=""></servo>						
Offset Voltage	VDAOF	-80	-	+80	mV	FDOUT,TDOUT,SDOUT,CLVOUT
Maximum Output Voltage	VDAH	0.8	1.2	-	V	FDOUT,TDOUT,SDOUT,CLVOUT
Minimum Output Voltage	VDAL	-	-1.2	-0.8	V	FDOUT,TDOUT,SDOUT,CLVOUT
<bias amplifier=""></bias>			1			
Maximum Output Current	IBO	-	±1.5	-	mA	VBIAS, BIAS Fluctuation: 200mV or less
<rf amplifier=""> Offset Voltage</rf>	VRFOF	-	0	_	mV	AC,BD,EQO
Maximum Output Voltage	VRFH	1.0	1.2	-	V	AC,BD,EQO
Minimum Output Voltage	VRFL	-	-1.3	-1.1	V	AC,BD,EQO
<fe amplifier=""></fe>						
Offset Voltage	VFEOF	-	0	-	mV	AC,BD,ANA MONIO,ANA MONI1
Maximum Output Voltage	VFEH	1.0	1.4	-	V	AC,BD,ANA_MONI0,ANA_MONI1
Minimum Output Voltage	VFEL	-	-1.4	-1.0	V	AC,BD,ANA_MONI0,ANA_MONI1
<te amplifier=""></te>	1					
Offset Voltage	VTEOF	-	70	-	mV	E,F,ANA_MONI0,ANA_MONI1
Maximum Output Voltage	VTEH	1.0	1.4	-	V	E,F,ANA_MONI0,ANA_MONI1
Minimum Output Voltage	VTEL	-	-1.4	-1.0	V	E,F,ANA_MONI0,ANA_MONI1
<asymmetry amplifier=""></asymmetry>		-				
Offset Voltage	VASYOF	-	0	-	mV	ASY=VBIAS,RFI,ANA_MONI0
Maximum Output Voltage	VASYH	1.1	1.4	-	V	ASY,RFI,ANA_MONI0
Minimum Output Voltage	VASYL	-	-1.4	-1.1	V	ASY,RFI,ANA_MONI0
<apc block=""></apc>					1	DD 2112
Output Voltage 1	VAPC1	2.4	2.8	-	V	PD="H", LD,ANA_MONI0
Output Voltage 2	VAPC2	-	0.1	0.5	V	PD="L", LD,ANA_MONI0
Maximum Reference Voltage	VAPCH	ī	220	-	mV	PD,LD,ANA_MONI0
Minimum Reference	VAPCL	-	145	-	mV	PD,LD,ANA_MONI0

### **Application Information**

### Power on/ Reset Timing/ Power off

Release the Reset Signal by L input with over 100µs after clock input from I/O pins of 16.9344MHz becomes stable. (See Figure 4)

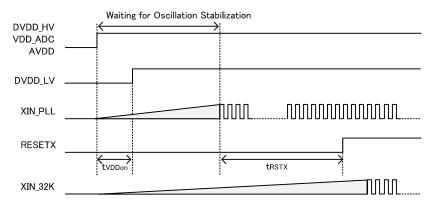


Figure 4. Power on/ Reset Timing

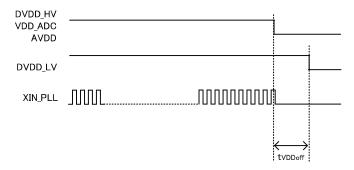


Figure 5. Power off

Davamatav	Symbol		Rating	Llmit	Remarks	
Parameter		MIN	TYP	MAX	Unit	Remarks
Time lag of Power Supply at Starting	tVDDon	0	-	-	ms	
Reset L Interval	tRSTX	100	-	-	μs	
Time lag of Power Supply at Shutting down.	tVDDoff	0	-	-	ms	

Note) There is a risk that the electric current flows in case the order of power supply starting and shutting down is other than the above order.

### **Oscillation Stable Time**

Suggested value for XIN\_PLL(16.9344MHz) oscillation stable time is 4ms.

Suggested value for XIN\_32K(32.768kHz) oscillation stable time is 500ms.

The above-mentioned oscillation stable time cannot be guaranteed since the oscillation stable time depends on crystal oscillator, external constant, or board layout. Check the oscillation stable time of your own system.

# I/O Equivalence Circuits

No.	Name	I/O	Power	Internal Circuits	No. Name	I/O	Power	Internal Circuits
1	RESETX	I	DVDD_HV	\$-13+-13+0	2 SD_WP 4 SD_CON 5 SD_DAT1 6 SD_DAT0 7 SD_CLK 8 SD_CMD 9 SD_DAT3 10 SD_DAT2	I I/O I/O O O I/O I/O	DVDD_HV	
36 37 38 39 40 41 43 44 47 48 61 62	ADINO ADIN1 ADIN2 ADIN3 ADIN4 ADIN5 ADIN6 ADIN7 ANA_MONI0 ANA_MONI1 AD_MONI0 AD_MONI1 FDOUT TDOUT SDOUT CLVOUT	I I I I I I O O O O	VDD_ADC		13 GPIO0_8 14 GPIO0_9 15 GPIO0_10 21 MSCS 22 MSDI 23 MSCLK 24 MSDO 25 SSCS 26 SSDI 27 SSCLK 28 SSDO 29 GPIO0_19 30 GPIO0_20 31 GPIO0_21 32 GPIO0_22 65 CLK88	I/O I/O O O I O O I I O I/O I/O I/O O		
45	RFI	I	AVDD		72 DSDLO 73 DSDRO 74 DSDBCKO 77 MCLKO 81 DATAO0 82 BCKO 83 LRCKO 84 DATAO1	I/O I/O I/O O O O		
46	EQO	0	AVDD		93 GPIO1_7 94 GPIO1_8 95 GPIO1_9 101 UARTO_RXD 102 UARTO_TXD 103 UARTO_RTS 104 UARTO_CTS 105 GPIO1_14 106 GPIO1_15	I/O I/O I/O I O O I I/O I/O		
	AC BD	I	AVDD		107 GPIO1_16 108 GPIO1_17 109 GPIO1_18 110 LRCKI0 111 BCKI0 112 DATAI0 113 LRCKI1	I/O I/O I/O I I I I		
54 55		I	AVDD		114 BCKI1 115 DATAI1 116 UART1_RTS 117 UART1_CTS 120 RCR 121 UART1_RXD 122 UART1_TXD	I I I/O I/O I I O		

Figure 6. I/O equivalence circuits 1

# I/O Equivalence Circuits – continued

No.	Name	I/O	Power	Internal Circuits	No.	Name	I/O	Power	Internal Circuits
56 57	PD	I O	AVDD		75 76 118	SCL0 SDA0 SCL1 SDA1	I/O I/O I/O I/O	DVDD_HV	
58	ASY	I	AVDD	#	88 89 90 91	FL_DAT2 FL_DAT1 FL_CS FL_DAT3 FL_CLK FL_DAT0	I/O I/O O I/O O I/O	DVDD_HV	
52	VBIAS	0	AVDD	#	98		I/O	DVDD <u>-</u> HV	100,2M
59 60	PCO FCO	0 0	AVDD		100	REXTI	I	DVDD_HV	
					124 125	XIN_32K XOUT_32K	0	DVDD_HV	201/230K
66	JTAG_TDO	0	DVDD_HV		127	XIN_PLL	I		
67	JTAG_TCK	I		↑ <del> </del>	128	XOUT_PLL	Ö	DVDD_HV	NOUTUL NOUTUL
68 69 70	JTAG_TMS JTAG_TDI JTAG_TRST TMODE	I I I	DVDD_HV						

Figure 7. I/O equivalence circuits 2

### **Operational Notes1**

About Compatibility in USB Memory Device and SD Memory Card
 According to the file structure and communication speed of USB memory, SD memory card, this LSI might not play
 back correctly.

### 2. About Compatibility in Bluetooth device

According to the type of Bluetooth device, , this LSI might not play back correctly.

### 3. About 2X Speed Recording

Recording to a memory with slow access speed may require data connection operation. 2X speed recording to all the memories cannot be guaranteed.

### 4. Power OFF or Memory Disconnection Under Memory Writing

The sudden power off or memory disconnection during recording or file write operation to a memory may break the data in a memory.

### 5. Browsing Operation

With a memory with slow access speed, browsing operation during music playing may generate skipping.

### 6. CD-ROM Playing

CD-ROM playing operation is premised on data being inputted so that an internal data buffer may not become empty. When an input does not meet the deadline and internal data buffers become empty, skipping occurs.

#### 7. Playing Time of MP3 File

The playing time when MP3 file playing may shift when fast forward playing, rewind playing, and VBR playing.

### 8. Write-In Operation Exceeding Memory Size

Writing to a file when memory size is exceeded is not supported.

# 9. Write-In Operation of the File Size Exceeding FAT Specification

Writing to a file when file size is exceeded is not supported.

### 10. About I2C Format I/F

Although this LSI has adopted the I2C format, the level shifter circuit is not built in.

For this reason, level shifter is needed for connection with the device besides the range of operating power supply voltage of this LSI.

### 11. CD Media Playing

According to the condition of CD media, flawed, dirty, curved, eccentric and etc., this LSI might not play back normally.

#### 12. Application Block Diagram

Each software function of Audio Encoder, Audio Decoder, BT stack A2DP, SBC Decoder and File System(FTA12/16/32, ISO9660) described in Figure 1. Application Block are realized by downloading applicable program from external Serial Flash ROM.

### **Operational Notes2**

#### Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### Operational Notes2 - continued

#### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

#### 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

### 12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

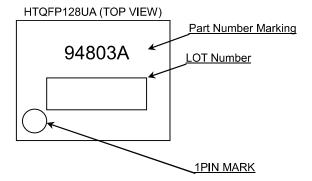
### 13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

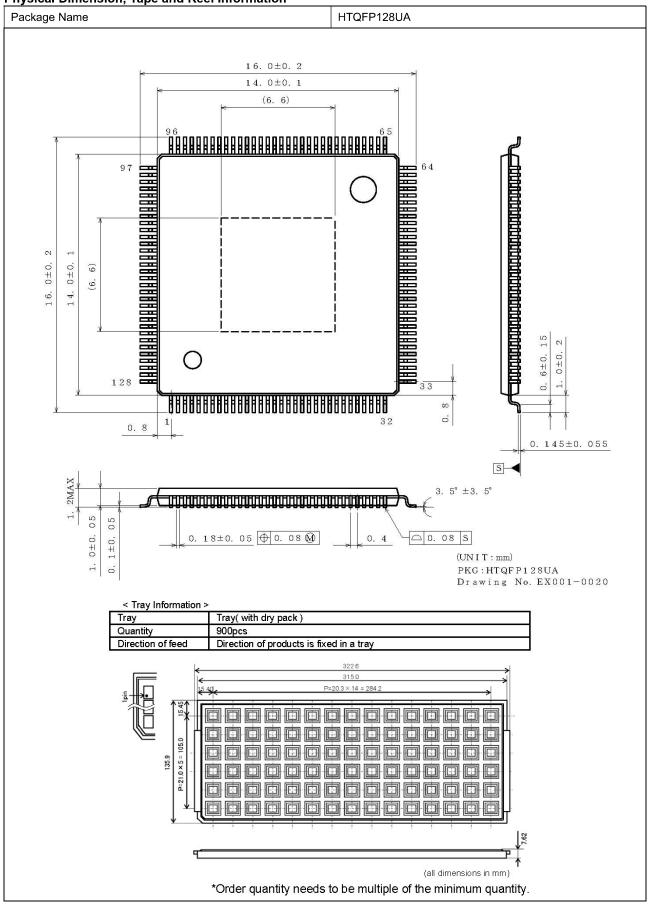
# **Ordering Information**



# **Marking Diagram**



Physical Dimension, Tape and Reel Information



# **Revision History**

Date	Revision	Changes
30.Aug.2016	001	New Release
25.Jan.2017	002	P10: Modified Block name of 118/119pin to I2C. P11: Modified pin name of Serial Flash ROM from SCLK to SIO3. P14: Modified pin name FLAG1 to GPIO1_7, FLAG2 to GPIO1_8, VC to VBIAS, and removed ASY_TEST, APCREF in Electrical Characteristics. P18: Added Note about Application Block diagram.

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(Note1) Medical Equipment Classification of the Specific Applications

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CLASSIV	CLASSIII	CLASSⅢ	CLASSIII	

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