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Replacing the 73S8014R with the 73S8014BL

1 Introduction

This document describes how to replace the Teridian 73S8014R smart card interface IC with the Teridian 73S8014BL. The 73S8014BL is a cost-optimized derivative of the 73S8014R smart card interface device. This is achieved by removing non-essential functions of the 73S8014R. These differences are discussed and various precautions are examined to insure the proper transition to the 73S8014BL. In addition, a dual footprint implementation is described using the 73S8014R and 73S8014BL.

This document is intended for both the hardware and software application developer that currently uses the Teridian 73S8014R smart card interface device. Knowledge of the ISO-7816 is required.

2 Feature Modifications and Removals

Several features available in the 73S8014R have been removed or redefined to achieve the lowest cost interface device possible while adding card switch debounce and power down. The reason for removal of some of these features is to enable the use of a package that has the smallest possible pin count and therefore the lowest possible cost. This combination of redefinition and removal of these features allows the removal of 6 pins. The 20-pin 73S8014R can now be replaced by the 14-pin 73S8014BL.

2.1 Removal of the AdjustableVDD Fault

The 73S8014R has a pin named VDDF_ADJ. This pin allows the threshold for the VDD fault circuit to be adjusted to a desired voltage. In order to reduce the number of pins, this feature has been removed in the 73S8014BL. The fault circuit is still implemented, but the adjustability has been removed. The VDD default threshold is set internally at 2.3 V.

2.2 Removal of the Clock Divider

The 73S8014R uses two input pins, CLKDIV1 and CLKDIV2, to select among the four clock divider rates of divide by 1, 2, 4 and 8. Table 1 shows the clock divider rates for the CLKIN1 and CLKIN2 input pins.

Table 1: 73S8014R CLKDIV1 and CLKDIV2 Usage

CLKDIV1	CLKDIV2	CLK
0	0	⅛ XTALIN
0	1	¼ XTALIN
1	0	XTALIN
1	1	½ XTALIN

In order to remove two input pins from the 73S8014R, the clock divider circuit on the 8014B has been removed and internal clock divider is fixed at a divide by 2 rate.

2.3 Removal of XTALOUT Pin

The pin XTALOUT pin of the 73S8014R has been removed so the smart card clock source must be provided externally to the XTALIN pin.

3   Feature Enhancements

The 73S8014BL includes some feature enhancements not found on the 73S8014R.

3.1   PRES Input Debounce

The 73S8014R has no debounce on the PRES input. As a result, it is possible to see bounce on the $\overline{\text{OFF}}$ output when a card is inserted or removed. The 73S8014BL has added a debounce circuit. The operation of the debounce is different depending on whether the card is inserted or removed. The reason for the difference on the card event is due to action required upon a card removal when the card was activated before removal. A debounce period is not desired in this case as the emergency deactivation must be handled immediately to insure that no data corruption on the card is allowed to occur while the card is being removed. The $\overline{\text{OFF}}$ output will immediately go low on the falling edge of PRES and stay low until the PRES input is solidly high for 5 ms. In the case for a card insertion, the debounce period is approximately 5 ms, meaning that the PRES input is solidly high for this amount of time.   After 5 ms of having PRES solidly high has elapsed, the $\overline{\text{OFF}}$ output will go high.

3.2   Power Down

The 73S8014R has no low-power operation mode. The analog circuitry and oscillators are always powered and running therefore drawing power whether the card is activated or not. The 73S8014BL adds low-power capability without the addition of a separate power down pin. The power down mode is only available outside a card session and is initiated by setting the RSTIN pin high when both $\overline{\text{CMDVCC}}$ and 5V/$\overline{\text{3V}}$ are high. Power down is not immediately entered upon this condition, but if it is held for 2 ms, then the 8014B will enter the power down mode. The power down mode will draw about 1 µA on VPC and VDD.

To exit from power down, the RSTIN input must be taken low. The $\overline{\text{CMDVCC}}$ and 5V/$\overline{\text{3V}}$ have no effect when exiting from power down. When RSTIN is taken low, the $\overline{\text{OFF}}$ output immediately goes low for about 5 to 7 ms to indicate to the host that the 73S8014BL is exiting from power down. This is necessary to allow all the circuits and oscillators to restart and stabilize. After this time has elapsed, the $\overline{\text{OFF}}$ output will reflect the card status. If the card is inserted, then activation can begin.

The card detection logic is available when the 73S8014BL is in power down mode. The debounce circuit operates the same whether in or out of power down.

4   Firmware Precautions

When transitioning from the 73S8014R to the 73S8014BL, the control signal timing is nearly identical between the two devices, however the feature differences between the parts forces some of the control signals and timing to change. The following sections detail these differences and indicate where they may cause operational difficulties.

4.1   Holding RSTIN high outside a Card Session

When using the 73S8014R, the RSTIN input is a don't care when a card is deactivated or removed. This is not true for the 73S8014BL. The 73S8014BL uses RSTIN to control the power down mode under these conditions. If the RSTIN is set high while $\overline{\text{CMDVCC}}$ and 5V/$\overline{\text{3V}}$ are high and held for at least 2 ms, then the 73S8014BL will enter power down mode. The 73S8014BL will not be able to activate an inserted card when $\overline{\text{CMDVCC}}$ is set low if in power down mode. The RSTIN input must be taken low prior to activating a card to exit the power down mode and then wait until the device is ready before attempting to activate the card. See the *73S8014BL Data Sheet* for details on how to exit power down and determine when the 73S8014BL is ready to activate a card.

4.2   Activation with CLK Delay

Like the 73S8014R, the 73S8014BL can delay the start of the CLK output if the RSTIN is high at $\overline{\text{CMDVCC}}$ going low or at time t1 as described in the *73S8014BL Data Sheet*. Time t1 indicates a stable and valid VCC output as part of the activation sequence. If this CLK delay is used and the RSTIN input is high before the $\overline{\text{CMDVCC}}$ is taken low, then the time between RSTIN being set high and the time between $\overline{\text{CMDVCC}}$ being set low must not exceed 2 ms or the power down mode can be initiated if the 5V/$\overline{\text{3V}}$ input is set for 5 V operation (set high). If this time period is longer than 2 ms, then the 73S8014BL will go into power down and any falling edge of $\overline{\text{CMDVCC}}$ will be ignored.

4.3   3V VCC Activation

When the 73S8014R is being configured for 3 V operation, the 5V/$\overline{\text{3V}}$ should be low upon the falling edge of $\overline{\text{CMDVCC}}$ to generate 3 V on VCC. When activating the 73S8014R, the host software should have some setup time between the 5V/$\overline{\text{3V}}$ being set low and the falling edge of $\overline{\text{CMDVCC}}$ to start activation. However, the 73S8014R can actually power VCC at 3 V if the 5V/$\overline{\text{3V}}$ and $\overline{\text{CMDVCC}}$ fall at the same time. With the 73S8014BL, this will actually configure VCC to operate at 1.8 V. As a result, the 73S8014BL must have a setup time that must exceed 4 µs so the VCC will activate at 3.0 V.

4.4   Clock Divider

As described in Section 2.2, the clock divider configuration is different between the 73S8014R and the 73S8014BL. The 73S8014BL defaults the divider to divide by 2. If the 73S8014R configuration used any other divider rate than divide by 2, then external clock source must be changed such that it is twice the desired smart card clock frequency.

5   Dual Footprint Schematic and Layout

5.1   Schematic

If having a dual footprint layout able to support both the 73S8014R and 73S8014BL is desired, then the schematic shown in Figure 1 will accomplish this. This schematic allows for either the 73S8014R or 73S8014BL device to be used in a given application to allow for the greatest flexibility in manufacturing. Using this schematic and adhering to the firmware precautions in Section 4 allow the full interchangeability of using either the 73S8014R or 73S8014BL.
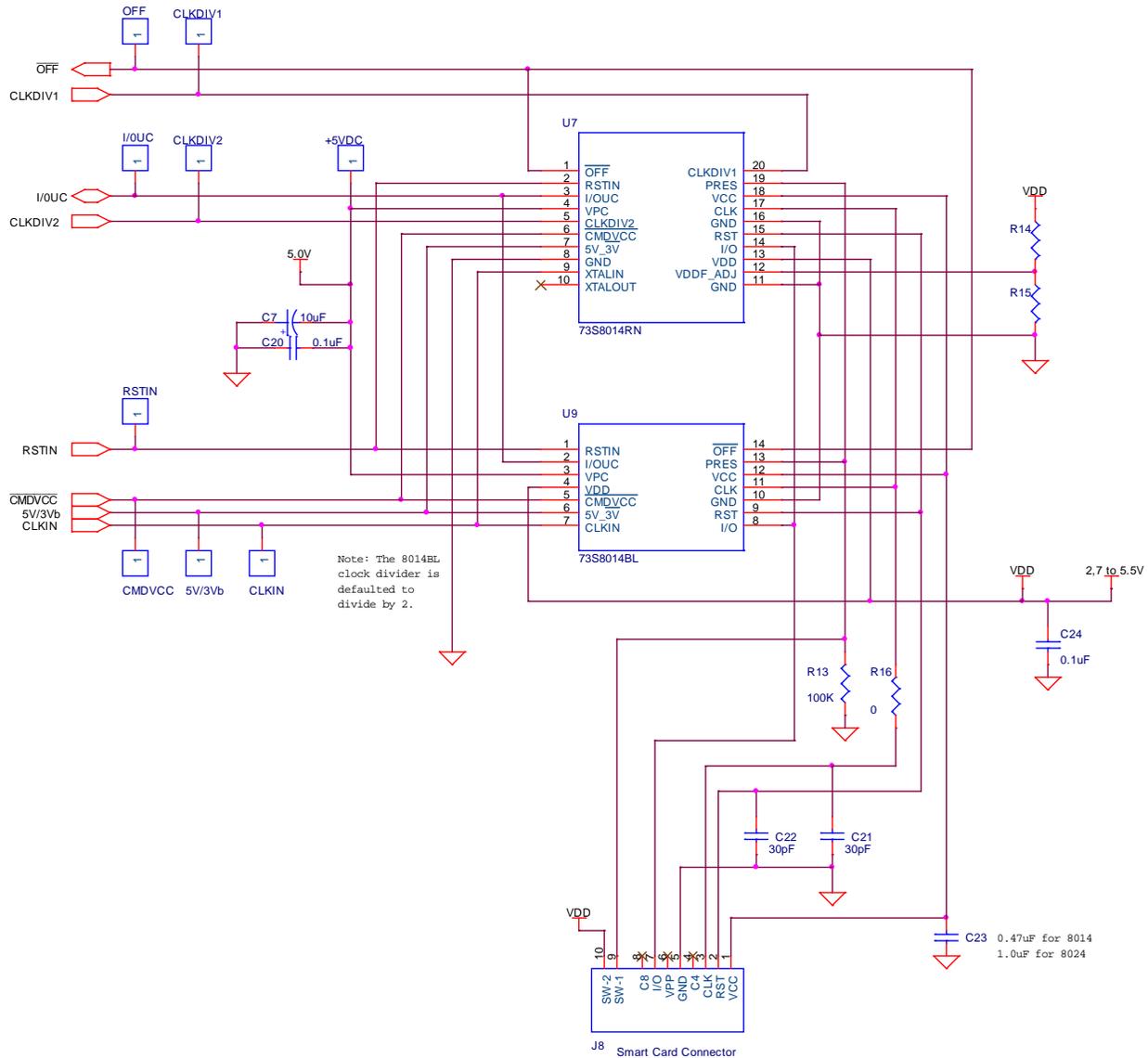

Figure 1: 73S8014R and 73S8014BL Dual Schematic

5.2 Layout

An example of a dual layout of the schematic shown in Figure 1 is shown in the following figures. The 73S8014R and 73S8014BL are shown overlapping each other on the top of the PCB and the smart card connector is on the bottom. The smart card connector used is a full size smart card connector with card detection switch used on all Teridian smart card evaluation boards. See any 73S80xx Evaluation Board User Guide for further details. Figure 2 shows the top and bottom silk screen with green showing the top and brown showing the bottom. The top layer is shown in Figure 3 and the bottom layer is shown in Figure 4.
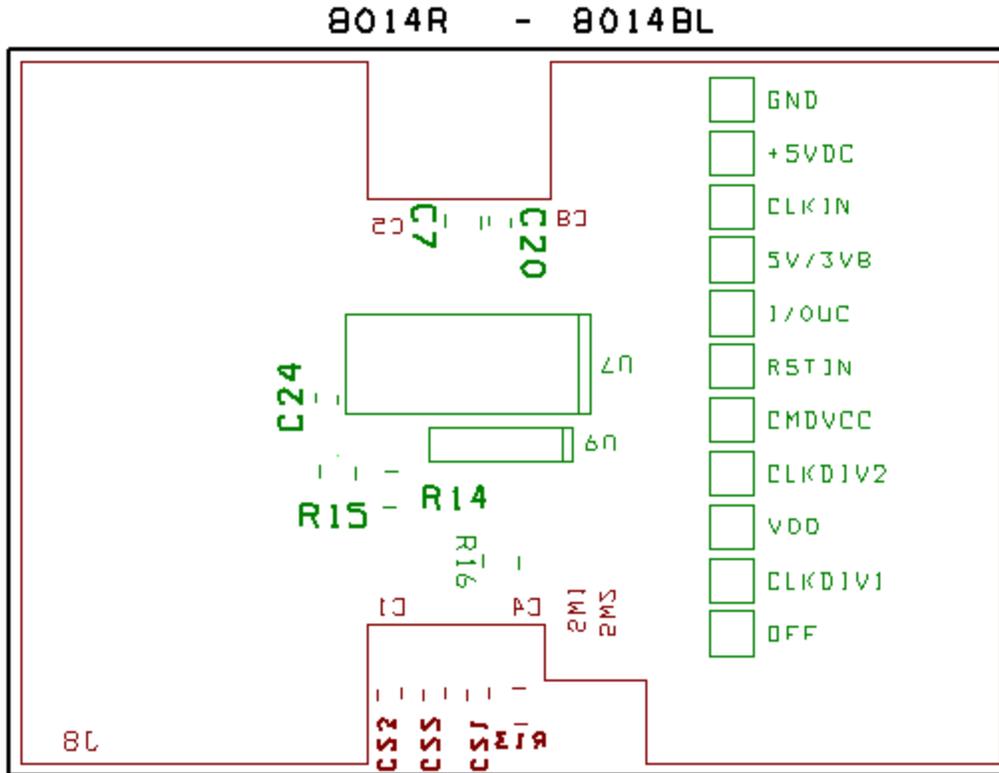

Figure 2: 73S8014R and 73S8014BL Dual Layout Top and Bottom Silk Screen
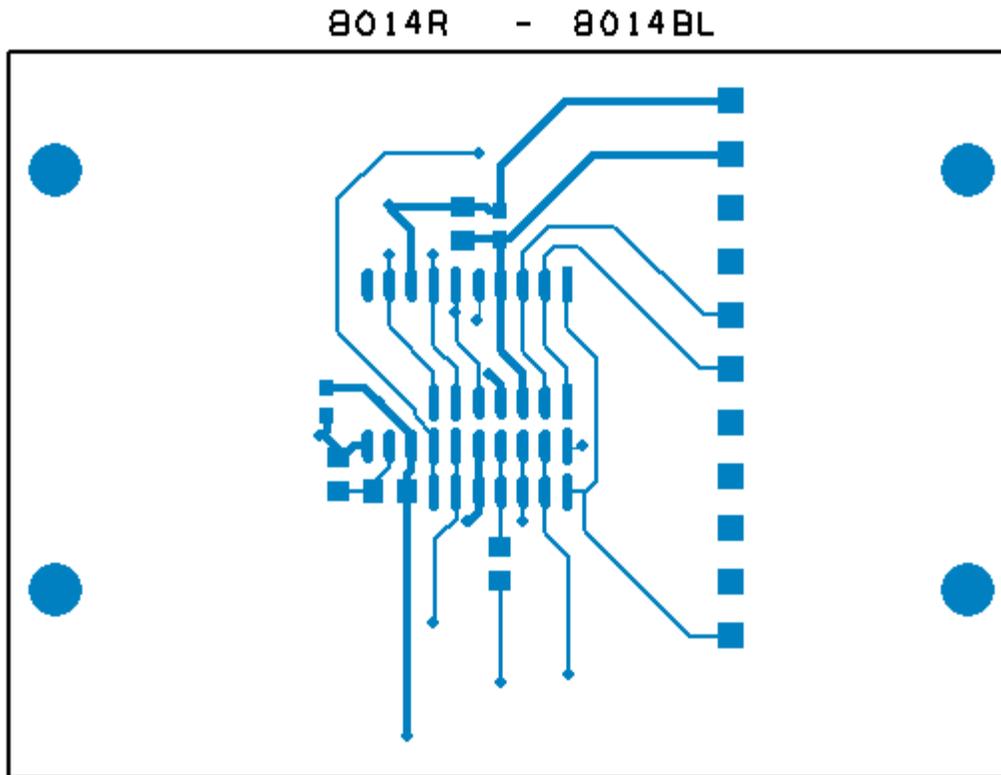
8014R   -   8014BL

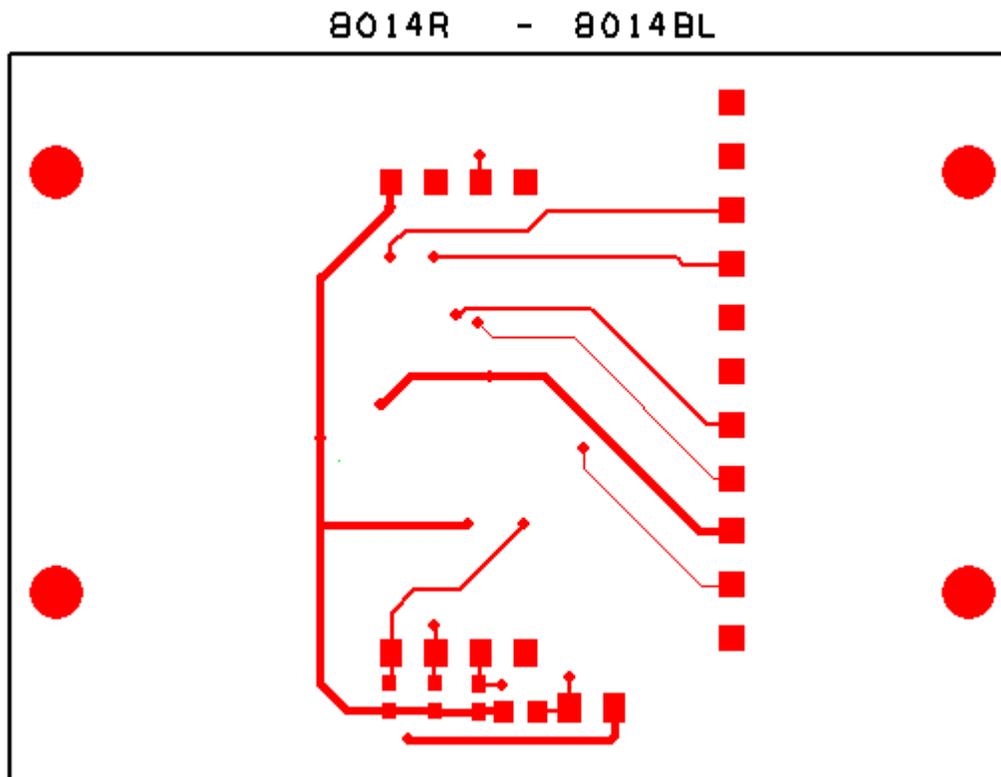
Figure 3: 73S8014R and 73S8014BL Dual Layout – Top Layer

8014R   -   8014BL

Figure 4: 73S8014R and 73S8014BL Dual Layout – Bottom Layer

Revision History

Revision	Date	Description
1.0	1/29/2010	First publication.